WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a plurality of transistors formed on a surface of said semiconductor substrate;

an interlayer insulating film for covering said transistors; and

a plurality of ferroelectric capacitors formed over said interlayer insulating film, an electrode of each of said plurality of ferroelectric capacitors being connected to one of a source or a drain of said transistor via a first contact plug,

wherein said plurality of ferroelectric capacitors are arranged in an array,

wherein each of said plurality of ferroelectric capacitor has substantially a rectangular planar shape, and

wherein the ratio between the length of a long side of the rectangular shape and the distance between the long sides of two ferroelectric capacitors adjacent to each other substantially coincides with the ratio between the length of a short side of the rectangular shape and the distance between the short sides of two ferroelectric capacitors adjacent to each other.

2. A semiconductor device comprising:

a semiconductor substrate;

a plurality of transistors formed on a surface of said semiconductor substrate;

an interlayer insulating film for covering said transistors;

a plurality of ferroelectric capacitors formed over said interlayer insulating film, an electrode of each of said plurality of ferroelectric capacitors being connected to one of a source or a drain of said transistor via a first contact plug; and

a plurality of bit lines formed over said interlayer insulating film, each of said plurality of bit lines being connected to the other one of the source or the drain of said transistor via a second contact plug;

wherein said plurality of ferroelectric capacitors are arranged in an array, and

wherein the first contact plug is located at substantial central point of a minimal rectangular shape made by four ferroelectric capacitors out of said plurality of ferroelectric capacitors.

3. The semiconductor device according to claim 1,

wherein a straight line connecting the source and the drain of said transistor extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors.

4. The semiconductor device according to claim 2,

wherein a straight line connecting the source and the drain of said transistor extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors.

5. The semiconductor device according to claim 3, further comprising an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions,

wherein each element region includes two transistors out of said plurality of transistors, and

wherein the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor.

6. The semiconductor device according to claim 4, further comprising an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions,

wherein each element region includes two transistors out of said plurality of transistors, and

wherein the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor.

7. The semiconductor device according to claim 3, further comprising an element isolation insulating

film formed on the surface of said semiconductor device and isolating a plurality of element regions,

wherein each element region includes two transistors out of said plurality of transistors, and

wherein the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor.

8. The semiconductor device according to claim 4, further comprising an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions,

wherein each element region includes two transistors out of said plurality of transistors, and

wherein the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor.

9. The semiconductor device according to claim 5,

wherein the other one of the source or the drain of said transistor is shared by said two transistors in each element region.

10. The semiconductor device according to claim 6,

wherein the other one of the source or the drain of said transistor is shared by said two transistors in each element region.

11. The semiconductor device according to claim 7,

wherein the other one of the source or the drain of said transistor is shared by said two transistors in each element region.

12. The semiconductor device according to claim 8,

wherein the other one of the source or the drain of said transistor is shared by said two transistors in each element region.

13. A semiconductor device comprising:

a semiconductor substrate;

a plurality of transistors formed on a surface of said semiconductor substrate;

an interlayer insulating film for covering said transistors;

a plurality of ferroelectric capacitors formed over said interlayer insulating film, an electrode of each of said plurality of ferroelectric capacitors being connected to one of a source or a drain of said transistor via a first contact plug; and

a plurality of bit lines formed over said interlayer insulating film, each of said plurality of bit lines being connected to the other one of the source or the drain of said transistor via a second contact plug,

wherein said plurality of ferroelectric capacitors are arranged in an array,

wherein each of said ferroelectric capacitors has substantially a rectangular planar shape, and

wherein the second contact plug is located between respective long sides of two adjacent ferroelectric capacitors out of said plurality of ferroelectric capacitors.

14. The semiconductor device according to claim 1,

wherein each of said ferroelectric capacitor has substantially a square planar shape, and

wherein distances between adjacent ferroelectric capacitors are substantially constant in any of longitudinal or latitudinal directions of arrays constituted by said ferroelectric capacitors.

15. The semiconductor device according to claim 2,

wherein each of said ferroelectric capacitor has substantially a square planar shape, and

wherein distances between adjacent ferroelectric capacitors are substantially constant in any of longitudinal or latitudinal directions of arrays constituted by said ferroelectric capacitors.

16. The semiconductor device according to claim 13,

wherein each of said ferroelectric capacitor has substantially a square planar shape, and

wherein distances between adjacent ferroelectric capacitors are substantially constant in any of

longitudinal or latitudinal directions of arrays constituted by said ferroelectric capacitors.

17. The semiconductor device according to claim 1,

wherein said ferroelectric capacitors has substantially a rectangular planar shape, and

wherein a distance between long sides of two adjacent ferroelectric capacitors is larger than the distance between short sides of two adjacent ferroelectric capacitors.

18. The semiconductor device according to claim 2,

wherein said ferroelectric capacitors has substantially a rectangular planar shape, and

wherein a distance between long sides of two adjacent ferroelectric capacitors is larger than the distance between short sides of two adjacent ferroelectric capacitors.

19. The semiconductor device according to claim 13,

wherein said ferroelectric capacitors has substantially a rectangular planar shape, and

wherein a distance between long sides of two adjacent ferroelectric capacitors is larger than the distance between short sides of two adjacent ferroelectric capacitors.

20. A semiconductor device comprising:

a semiconductor substrate;

a plurality of transistors formed on a surface of said semiconductor substrate;

an interlayer insulating film for covering said transistors; and

a plurality of ferroelectric capacitors formed over said interlayer insulating film, an electrode of each of said plurality of ferroelectric capacitors being connected to one of a source or a drain of said transistor via a first contact plug,

wherein each of said ferroelectric capacitors has substantially a circular planar shape.

21. A manufacturing method of a semiconductor device, comprising the steps of:

forming a plurality of transistors on a surface of a semiconductor substrate;

forming an interlayer insulating film for covering the transistors; and

forming a plurality of ferroelectric capacitors over the interlayer insulating film, an electrode of each of the plurality of ferroelectric capacitors being connected to one of a source or a drain of the transistor via a first contact plug,

wherein the plurality of ferroelectric capacitors are arranged in an array,

wherein each of the plurality of ferroelectric capacitors has substantially a rectangular planar shape, and

wherein the ratio between the length of a long side of the rectangular shape and the distance between the long sides of two ferroelectric capacitors adjacent to each other substantially coincides with the ratio between the length of a short side of the rectangular shape and the distance between the short sides of two ferroelectric capacitors adjacent to each other.

22. A manufacturing method of a semiconductor device, comprising the steps of:

forming a plurality of transistors on a surface of a semiconductor substrate;

forming an interlayer insulating film for covering the transistors;

forming a plurality of ferroelectric capacitors over the interlayer insulating film, an electrode of each of the plurality of ferroelectric capacitors being connected to one of a source or a drain of the transistor via a first contact plug; and

forming a plurality of bit lines over said interlayer insulating film, each of said plurality of bit lines being connected to the other one of the source or the drain of said transistor via a second contact plug,

wherein the plurality of ferroelectric capacitors are arranged in an array, and

wherein the first contact plug is located at substantial central point of a minimal rectangular

shape made by four ferroelectric capacitors out of the plurality of ferroelectric capacitors.

23. A manufacturing method of a semiconductor device, comprising the steps of:

forming a plurality of transistors on a surface of a semiconductor substrate;

forming an interlayer insulating film for covering the transistors;

forming a plurality of ferroelectric capacitors over the interlayer insulating film, an electrode of each of the plurality of ferroelectric capacitors being connected to one of a source or a drain of the transistor via a first contact plug; and

forming a plurality of bit lines over said interlayer insulating film, each of said plurality of bit lines being connected to the other one of the source or the drain of said transistor via a second contact plug,

wherein the plurality of ferroelectric capacitors are arranged in an array,

wherein each of the plurality of ferroelectric capacitors has substantially a rectangular planar shape, and

wherein the second contact plug is located between respective long sides of two adjacent ferroelectric capacitors out of the plurality of ferroelectric capacitors.

24. The manufacturing method of the semiconductor device according to claim 21,

wherein each of the plurality of ferroelectric capacitors has substantially a square planar shape, and

wherein distances between adjacent ferroelectric capacitors are substantially constant in any of longitudinal or latitudinal directions of arrays constituted by the ferroelectric capacitors.

25. The manufacturing method of the semiconductor device according to claim 22,

wherein each of the plurality of ferroelectric capacitors has substantially a square planar shape, and

wherein distances between adjacent ferroelectric capacitors are substantially constant in any of longitudinal or latitudinal directions of arrays constituted by the ferroelectric capacitors.

26. The manufacturing method of the semiconductor device according to claim 23,

wherein each of the plurality of ferroelectric capacitors has substantially a square planar shape, and

wherein distances between adjacent ferroelectric capacitors are substantially constant in any of longitudinal or latitudinal directions of arrays constituted by the ferroelectric capacitors.

27. The manufacturing method of the semiconductor device according to claim 21,

wherein each of the plurality of ferroelectric capacitors has substantially a rectangular planar shape, and

wherein a distance between long sides of two adjacent ferroelectric capacitors is larger than the distance between short sides of two adjacent ferroelectric capacitors.

28. The manufacturing method of the semiconductor device according to claim 22,

wherein each of the plurality of ferroelectric capacitors has substantially a rectangular planar shape, and

wherein a distance between long sides of two adjacent ferroelectric capacitors is larger than the distance between short sides of two adjacent ferroelectric capacitors.

29. The manufacturing method of the semiconductor device according to claim 23,

wherein each of the plurality of ferroelectric capacitors has substantially a rectangular planar shape, and

wherein a distance between long sides of two adjacent ferroelectric capacitors is larger than the distance between short sides of two adjacent ferroelectric capacitors.

30. A manufacturing method of a semiconductor device, comprising the steps of:

forming a plurality of transistors on a surface of a semiconductor substrate;

forming an interlayer insulating film for covering the transistors; and

forming a plurality of ferroelectric capacitors over the interlayer insulating film, an electrode of each of the plurality of ferroelectric capacitors being connected to one of a source or a drain of the transistor via a first contact plug,

wherein each of the plurality of ferroelectric capacitors has substantially a circular planar shape.